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Review
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A REVIEW OF DIGITAL PHASE SHIFTER ARCHITECTURES: OPERATING PRINCIPLES, COMPARISON METHODOLOGY, AND DESIGN TRADE-OFFS

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Abstract: Digital phase shifters are key components in modern wireless communication and sensing systems, including phased-array antennas, radar front ends, satellite terminals, and emerging mmWave/sub-THz platforms. However, the reported literature remains highly heterogeneous in terms of architecture, technology platform, operating frequency, and validation depth, which makes direct comparison difficult. This review systematically examines 27 papers covering a total of 30 digital phase-shifter designs and classifies them into four main categories: switch-type phase shifters (STPS), vector-sum/vector-modulator-based phase shifters (VSPS/VMPS), lattice/all-pass-network-based phase shifters, and special/other approaches such as delay-based and NEMS-related solutions. An evidence-aware comparison methodology is adopted to evaluate the reported studies using key metrics including RMS phase error, RMS amplitude error, insertion loss/gain, DC power consumption, area, operating band, and implementation technology. The comparison shows that nominal bit resolution alone is not a sufficient predictor of practical phase accuracy; instead, performance is more strongly influenced by architectural realization, parasitic-aware implementation, calibration strategy, and operating frequency. The reviewed results further indicate that passive STPS structures remain attractive for low-complexity and low-power applications, whereas vector-based architectures provide high resolution and calibration flexibility at the expense of higher power and implementation complexity. Lattice/all-pass-based structures remain relevant for wideband phase-flat operation, while delay-based approaches appear promising for sub-THz applications. Overall, the review does not support the existence of a universally optimal topology; rather, the most suitable solution depends on the dominant application constraint, such as accuracy, bandwidth, power, area, or scalability. The taxonomy, comparison framework, and cross-comparison presented in this work are intended to support more consistent evaluation and more informed topology selection in future digital phase-shifter research.

Keywords: Digital phase shifters, Phased-array antennas, Beamforming, Vector-sum phase shifters, RMS phase error, mmWave and sub-THz systems

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1. Introduction

Modern wireless communication and sensing systems, including 5G/6G networks, mmWave links, satellite terminals, and radar front ends, rely heavily on digital beamforming and electronically steerable antenna arrays (Brilhante et al., 2023; Lin et al., 2024). In such systems, phase shifters provide the controlled phase progression required across array elements, thereby enabling beam steering, multi-beam operation, and adaptive interference suppression (Mailloux, 2017).

A phase shifter is an RF building block that changes the phase of a signal by a desired amount while ideally maintaining constant amplitude. In phased-array systems, the main-beam direction is determined by the relative phase applied to each element, which governs how the radiated fields combine in space (Mailloux, 2017). In practice, however, array performance depends not only on achieving the intended phase states, but also on maintaining phase accuracy and amplitude consistency across states, since state-dependent errors can increase sidelobe levels and reduce on-target gain. For this reason, phase and amplitude behavior should be evaluated together (Coviello et al., 2016).

Among the available approaches, digital phase shifters are particularly attractive for large-array implementations because they support integration, repeatable state selection, and calibration-friendly operation. Their effective performance is ultimately governed by state consistency over frequency and amplitude stability across phase states, especially in wideband and high-frequency regimes (Coviello et al., 2016). Ideally, an N-bit digital phase shifter provides 2^N discrete phase states, with an ideal least significant bit given by equation 1,

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$$LSB=\frac{360^\circ}{2^N} \quad (1)$$

However, the literature on digital phase shifters remains highly diverse. Reported implementations differ substantially in architecture, technology platform (e.g., CMOS/SiGe, GaAs/GaN MMIC, planar/PCB, and NEMS-related approaches), and validation depth, ranging from measured results to post-layout/EM studies and schematic-level simulations (Kebe et al., 2025; Gharsalli et al., 2026). In addition, performance reporting is often inconsistent. While many studies emphasize nominal resolution or insertion loss/gain, other important metrics, such as RMS amplitude error and large-signal linearity, are not reported consistently, even though they strongly influence transmitter robustness and phased-array pattern quality (Coviello et al., 2016; Kebe et al., 2025).

Despite the large number of reported digital phase-shifter implementations, existing studies differ considerably in architecture, operating frequency, technology platform, validation depth, and reported performance metrics, making direct comparison across published designs difficult. Although several review papers summarize digital phase-shifter technologies from device, circuit, or application perspectives, they generally do not provide a unified taxonomy together with a systematic comparison framework that explicitly distinguishes phase-generation mechanisms, validation levels, and reporting consistency. As a result, identifying the relative advantages, limitations, and practical design trade-offs of different architectures remains challenging. This gap motivates the present review.

Motivated by these gaps, this review makes three main contributions. First, it proposes a taxonomy of digital phase-shifter families and summarizes their typical operating principles and trade-offs. Second, it establishes an evidence-aware comparison methodology that harmonizes the core performance metrics while distinguishing validation depth. Third, it presents a cross-comparison of 27 papers covering 30 digital phase-shifter designs using a unified dataset, with measured IC/MMIC results emphasized where available to support more reproducible interpretation.

The remainder of this paper is organized as follows. Section II presents the taxonomy and operating principles of the main digital phase-shifter families. Section III describes the comparison methodology and fairness criteria adopted in this review. Section IV provides the cross-comparison results and discusses the main trends observed across the dataset. Finally, Section V concludes the paper.

2. Taxonomy and Operating Principles

Figure 1 illustrates the proposed taxonomy adopted throughout this review. Based on the primary phase-generation mechanism, digital phase shifters are classified into four main categories: (A) switch-type phase shifters (STPS), (B) vector-sum/vector-modulator-based phase shifters (VSPS/VMPS), (C) lattice- and all-pass-network-based phase shifters, and (D) special or other approaches that fall outside the mainstream synthesis mechanisms (Kebe et al., 2025; Gharsalli et al., 2026).

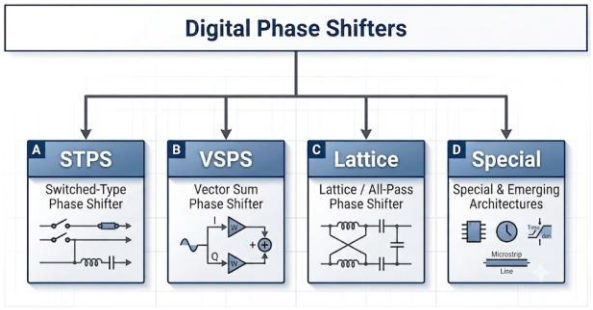


Figure 1. Proposed taxonomy of digital phase-shifter architectures based on the primary phase-generation mechanism.

2.1. Class A — Switch-Type Phase Shifters (STPS)

STPS architectures generate discrete phase states by switching among alternative signal paths or RF networks. Depending on the selected topology, the phase shift may be produced through switched-line, loaded-line, high-pass/low-pass, coupler-based, Schiffman, or related network arrangements.

Representative studies in this category include Anjos et al. (2020), Li et al. (2022), Chiu et al. (2021), Lin and Tsai (2022), Song et al. (2023), Zhan et al. (2024), Shen et al. (2025), Khazaei et al. (2025) and Kilinc et al. (2026). Li et al. (2022) proposed a compensated 7-bit GaAs pHEMT phase shifter for S-band applications, whereas Song et al. (2023) demonstrated a switched-filter GaN implementation operating at Ka-band frequencies. Lin and Tsai (2022) employed switched high-pass and low-pass T-networks in 65 nm CMOS, while Chiu et al. (2021) reported a low-loss GaN implementation emphasizing passive switched networks. Zhan et al. (2024) focused on broadband switched-path operation in advanced CMOS technology, whereas Shen et al. (2025) introduced a coupler-assisted switched architecture for W-band applications. Kilinc et al. (2026) retained the conventional switched-network operating principle while replacing grounded passive inductors with tunable active inductors, demonstrating that circuit-level innovations can improve integration density without altering the underlying STPS architecture. Khazaei et al. (2025) presented a modified Schiffman implementation for wideband operation, while Anjos et al. (2020) employed an all-pass-network-based switched architecture to improve bandwidth performance.

The main strengths of STPS designs are their high linearity, near-zero or zero static DC power consumption in the RF path, and relatively straightforward implementation in GaAs- or GaN-based technologies for high-power applications. However, their disadvantages become more pronounced as the target frequency and

resolution increase. In particular, layout parasitics at mmWave frequencies can degrade phase accuracy and introduce amplitude imbalance, while insertion loss typically increases with the number of bits and the complexity of the switched network.

2.2. Class B — Vector-Sum / Vector-Modulator-Based Phase Shifters (VSPS/VMPS)

In VSPS/VMPS architectures, the desired phase state is synthesized by weighting and recombining the in-phase (I) and quadrature (Q) signal components. This approach enables fine phase interpolation and, in active implementations, simultaneous gain adjustment. It is therefore particularly suitable for high-resolution and calibration-aware beamforming systems. Based on the classification adopted in Table 1, this category includes 10 papers and 11 distinct circuit implementations.

Representative examples include, Luo et al. (2019), Xiong et al. (2020), Wu et al. (2021), Shangguan et al. (2024), Tu et al. (2025), Minnella et al. (2025), Cho et al. (2025), Jiang et al. (2025), Wei et al. (2026), and Lee et al. (2026). Lee et al. (2026) proposed a BiCMOS vector-modulator architecture emphasizing low power consumption, whereas Minnella et al. (2025) demonstrated a compact 7-bit implementation in 28 nm FD-SOI CMOS. Cho et al. (2025) presented two independent 8-bit vector-modulator architectures operating around 140 GHz. Jiang et al. (2025) and Xiong et al. (2020) focused on broadband active vector-sum implementations, while Shangguan et al. (2024) demonstrated a high-frequency CMOS realization. Wei et al. (2026) achieved broadband operation over 2–18 GHz using active vector synthesis, whereas Wu et al. (2021) employed a passive vector-sum implementation with low RMS phase error. Tu et al. (2025) reported one of the lowest RMS phase errors in the dataset (0.18°–0.21°), and Luo et al. (2019) demonstrated wideband SiGe BiCMOS operation from 6 to 18 GHz.

The main advantages of Class B architectures are their high effective resolution, calibration flexibility, and potential for partial RF-loss compensation through gain. These properties make them well suited to modern beamforming arrays. Their limitations, however, include continuous DC power consumption, sensitivity to I/Q mismatch, and gain-phase coupling, all of which may require careful codebook design, calibration, or digital assistance.

2.3. Class C — Lattice / All-Pass-Network-Based Phase Shifters

The main objective of this class is to achieve a relatively flat phase response over a broad frequency range while maintaining nearly constant amplitude. This is typically pursued through lattice or all-pass-type network synthesis, where phase equalization and amplitude stability are jointly targeted.

Representative studies include Avci et al. (2019) and Taş and Kaçar (2025). Avci et al. (2019) demonstrated a CMOS symmetric-lattice phase shifter operating over 7.5–13 GHz, whereas Taş and Kaçar (2025) proposed a 3-bit LC symmetric-lattice phase shifter for 4.5–5.5 GHz applications with very low phase error. Although the number of studies in this category is relatively limited, lattice-based architectures remain attractive whenever phase flatness across bandwidth is prioritized.

It should be noted that several Class A architectures, including those reported by Anjos et al. (2020), Chiu et al. (2021), Lin and Tsai (2022), Zhan et al. (2024), and Khazaei et al. (2025), also incorporate all-pass or transmission-network sections. However, these networks function as switched RF paths rather than true lattice-based phase synthesis. Similarly, Wu et al. (2021) and Wei et al. (2026) employ passive RF networks but generate phase through vector synthesis and are therefore classified under Class B. Accordingly, the proposed taxonomy is based on the primary phase-generation mechanism, rather than the individual passive building blocks used in the implementation.

Class C implementations are valued for their wideband phase flatness and their potential to provide IC-compatible solutions at moderate frequencies. At the same time, their performance is strongly influenced by the quality factor (Q) of passive components, especially inductors and capacitors. As frequency increases, passive loss and switch parasitics make it more difficult to preserve ideal all-pass behavior, often leading to larger amplitude variation and reduced RF efficiency.

2.4. Class D — Special / Other Approaches

Class D comprises specialized implementations that cannot be directly categorized as conventional STPS, VSPS/VMPS, or lattice/all-pass architectures. These include delay-based solutions, NEMS transmission-line implementations, enabling circuit blocks, and system-level demonstrations.

Representative examples include Hamidi et al. (2019), Lin and Lin (2025), Ghorbani (2025), Uchino et al. (2025), and Sindhuja et al. (2025). Lin and Lin (2025) demonstrated a system-level implementation using a commercial phase-shifter module, whereas Ghorbani (2025) presented an RF-switch building block intended to enable future phase-shifter implementations. Uchino et al. (2025) proposed a delay-based architecture achieving 0.1° phase resolution at 150–160 GHz, while Sindhuja et al. (2025) investigated a NEMS transmission-line implementation with near-zero static power consumption. Hamidi et al. (2019) demonstrated a planar passive phase shifter intended for radar applications.

Although these studies address different implementation levels, they represent emerging design directions that extend beyond conventional digital phase-shifter architectures.

3. Comparison Methodology

IEEE Xplore, ScienceDirect, SpringerLink, Wiley Online Library, MDPI, and Google Scholar were used in the literature search. The terms "digital phase shifter," "switch-type phase shifter," "vector-sum phase shifter," "vector-modulator phase shifter," "lattice phase shifter,"

"all-pass phase shifter," "mmWave phase shifter," "sub-THz phase shifter," and "beamforming" were combined. Studies published between 2019 and 2026 were the main focus of the search; previous works were included where they offered a crucial benchmark or represented a basic architecture.

Studies were included in the quantitative comparison if they: (i) presented a digital phase-shifter circuit, system, or enabling architecture; (ii) reported sufficient quantitative information on operating frequency, phase resolution, insertion loss or gain, phase error, power consumption, implementation technology, or physical area; and (iii) provided a validation level that could be identified as measured, post-layout/EM simulated, schematic-level simulated, system/COTS demonstrated, or enabling-block based. Studies were excluded if they addressed only analog phase control, antenna-array behavior without phase-shifter-level data, or conceptual designs without sufficient quantitative performance information. Review papers were used only to support the background discussion and taxonomy development and were not included in the quantitative comparison presented in Table 1.

The final dataset comprised 27 papers and 30 distinct digital phase-shifter designs. Multiple designs reported within a single publication were treated as separate entries when they used different circuit architectures or produced independently reported performance results.

To improve the fairness of cross-study comparisons, the validation level of each design is explicitly indicated in Table 1 using standardized labels: [M] for measured results, [PL] for post-layout/EM simulation, [S] for schematic-level simulation, [NM] for numerical modeling, [SYS] for system-level demonstration, and [EB] for enabling-block studies.

Because the reviewed studies differ substantially in architecture, technology platform, operating frequency, and validation depth, a direct one-to-one comparison can easily become misleading. To improve consistency and interpretability, the comparison in this review was carried out using a multi-metric and evidence-aware framework. The goal was not to rank all studies using a single figure of merit, but rather to compare them in a way that preserves the architectural context and practical meaning of the reported results.

3.1. Performance Metrics and Definitions

The comparison was based primarily on the performance metrics most frequently reported across the literature and most relevant to phased-array operation.

3.1.1. RMS phase error

Phase accuracy was treated as one of the most critical performance indicators, since it directly affects beam pointing quality, sidelobe behavior, and array coherence. The reviewed dataset spans a wide range of reported values, from relatively high errors in schematic-level or lower-complexity designs to very low RMS phase errors in highly optimized measured implementations.

3.1.2. RMS amplitude error

RMS amplitude error was included to reflect the consistency of signal magnitude across phase states. This metric is important because phase accuracy alone does not guarantee satisfactory array-level behavior; amplitude imbalance can also distort the radiation pattern and reduce effective gain. When reported, lower RMS amplitude error was interpreted as more stable amplitude behavior across states.

3.1.3. Insertion loss (IL) or gain

For passive architectures such as many STPS and lattice-based designs, insertion loss is a primary concern because it directly affects link budget and may require additional RF gain elsewhere in the chain. For active vector-based architectures, gain can partially compensate internal RF loss, but this advantage must be interpreted together with power consumption, linearity, and state-dependent gain variation. For this reason, IL and gain were not treated as interchangeable quantities, but were interpreted according to the operating principle of each class.

3.1.4. DC power consumption (P_{dc})

Power consumption was treated as a key metric, especially for dense phased arrays, mobile terminals, and satellite systems, where replication across many channels makes per-element power especially important. At the same time, zero or low DC power at the phase-shifter level was not automatically interpreted as a system-level advantage, since high insertion loss may shift the burden to later gain stages.

3.2. Technology and Area Benchmarking

Process technology and physical footprint were also included in the comparison because both strongly influence implementation feasibility and performance trade-offs.

3.2.1. Technology platform

The reviewed studies span a wide range of technologies, including advanced CMOS and FD-SOI nodes, SiGe/BiCMOS platforms, GaAs/GaN MMIC processes, and larger PCB or planar implementations. These choices affect passive quality factor, switch parasitics, achievable integration density, and suitability for different frequency ranges. Accordingly, technology was interpreted not merely as a fabrication detail, but as an important contributor to the reported performance.

3.2.2. Physical area

Occupied area was considered because it directly affects scalability in multi-channel phased-array systems, especially at mmWave frequencies where element count is high and chip area is costly. However, area was not interpreted in isolation. A compact implementation may rely on aggressive technology scaling or active circuitry, whereas a larger implementation may reflect a different topology choice, a lower-cost platform, or a broader-band passive realization. Therefore, area comparisons were made in conjunction with architecture, operating band, and technology node.

3.3. Frequency-Band Categorization

To reduce the risk of misleading comparisons across fundamentally different operating conditions, the reviewed designs were also grouped according to frequency range. This step is important because the dominant nonidealities change significantly with frequency. For example, passive loss, device parasitics, layout sensitivity, and achievable Q factors differ substantially between sub-10 GHz, mmWave, and sub-THz implementations.

Accordingly, the reviewed studies were interpreted within three broad frequency categories:

Low/mid-frequency range (<10 GHz): typically associated with S-band and C-band applications.

mmWave range (24–100 GHz): relevant to radar, satellite links, and 5G/6G front ends.

Sub-THz range (>100 GHz): representing emerging high-frequency research scenarios with increasingly severe implementation constraints.

This grouping does not eliminate all comparison difficulties, but it improves fairness by reducing the chance of equating designs that operate under substantially different physical and technological constraints.

4. Results and Cross-Comparison

The 30 digital phase-shifter (DPS) designs covered by the 27 reviewed papers are compared in this section in terms of their architectural choices, technology platforms, and design objectives. The aim is not to identify a single best approach, but to clarify how different topologies redistribute the trade-offs among resolution, phase accuracy, bandwidth, insertion loss, chip area, and power consumption. Accordingly, the comparison is organized around the main trade-offs observed across the dataset rather than around isolated performance claims.

4.1. Resolution–Accuracy Relationship

A common assumption in the DPS literature is that increasing bit resolution improves phase accuracy by reducing phase quantization error. However, the reviewed results show that higher resolution does not always lead to lower RMS phase error at the circuit level. In practice, the relationship between resolution and accuracy is strongly influenced by architectural class, operating frequency, and the use of calibration or optimization techniques.

This trend can be observed by comparing the 7-bit implementations reported by Wu et al. (2021), Tu et al. (2025), and Minnella et al. (2025). Tu et al. (2025) reported an RMS phase error of only 0.18°–0.21°, whereas Minnella et al. (2025), despite employing the same nominal 7-bit resolution, reported phase errors of approximately 2.7°–4.7°. Wu et al. (2021) achieved RMS phase errors below 2.1° using a passive vector-sum topology. These results demonstrate that practical phase accuracy depends not only on nominal bit resolution but also on architectural realization, calibration strategy, implementation technology, and operating frequency.

A similar limitation of resolution-based interpretation can be observed at very high frequencies. Reference Uchino et al. (2025) uses a fine-resolution delay-based method and reports a phase error of 0.68° at 150–160 GHz. This result is notable not only because of its low reported error, but also because it is achieved in a frequency range where layout sensitivity, parasitics, and device mismatch make high-resolution systems increasingly fragile. This suggests that, at sub-THz frequencies, delay-based Class D methods may offer a more robust solution than conventional I/Q-based approaches, whose theoretical resolution advantage may be weakened by practical nonidealities.

Taken together, these findings show that resolution should not be interpreted independently of how it is implemented. In many cases, a lower-complexity architecture supported by selective optimization or frequency-appropriate synthesis may deliver more practically useful accuracy than a high-bit design without calibration.

4.2. Power Consumption and Area Trade-Offs

Area and power consumption remain key constraints in phased-array and highly integrated front-end systems, where element count, channel replication, and thermal density are critical. However, the reviewed studies show that these two metrics do not necessarily improve simultaneously. Compact implementations often rely on advanced process nodes or active circuitry, whereas passive zero-power solutions may introduce penalties elsewhere in the system.

Technology scaling contributes significantly to area efficiency, although architecture and passive-network complexity remain equally important. For example, Minnella et al. (2025) implemented a 7-bit vector-modulator phase shifter occupying only 0.33 mm^2 in 28 nm FD-SOI CMOS. By comparison, Lee et al. (2026) reported approximately 1.75 × 1.11 mm^2 in 130 nm BiCMOS, whereas Luo et al. (2019) occupied 1.8 × 1.3 mm^2 in 0.13 μm SiGe BiCMOS. These examples indicate that process scaling improves integration density, but the observed area differences are also influenced by architectural complexity and passive-network implementation.

Several passive implementations report zero or approximately zero static DC power consumption. Examples include the GaN STPS designs of Chiu et al. (2021) and Song et al. (2023), the passive vector-sum phase shifter of Wu et al. (2021), the planar microstrip implementation of Hamidi et al. (2019), and the APN-based STPS of Anjos et al. (2020). The NEMS-based transmission-line implementation of Sindhuja et al. (2025) also reports approximately zero static power consumption.

However, zero static power at the phase-shifter block does not necessarily correspond to minimum system-level energy consumption. Passive phase shifters may introduce considerable insertion loss, which increases the gain and power requirements of the surrounding RF

chain. By comparison, relatively low-power active implementations such as Tu et al. (2025), with a reported power consumption of 10 mW, and Lee et al. (2026), with 15.8 mW, may reduce the need for additional loss-compensation stages. Therefore, block-level DC power consumption and system-level energy efficiency should be evaluated separately.

4.3. Bandwidth and Loss Mechanisms

The reviewed studies also show that wide operating bandwidth is rarely achieved without cost in insertion loss, chip size, or implementation complexity. Increasing bandwidth should therefore be understood not as a free improvement, but as a design choice that redistributes penalties among other performance metrics.

The bandwidth–loss trade-off can be observed by comparing wideband implementations based on different phase-generation mechanisms. Anjos et al. (2020) reported an APN-based STPS operating over 14–50 GHz. Its insertion loss was approximately 7.4 ± 0.26 dB at 28 GHz and increased to 10 ± 0.22 dB at 39 GHz. By contrast, Wei et al. (2026) employed an active vector-sum architecture over 2–18 GHz and reported a gain of 1.5–3.2 dB. However, this active implementation consumed 105 mW and occupied approximately 1.24 × 0.86 mm^2. These examples show that wideband operation can be achieved through different architectural strategies, but the corresponding penalty may appear as insertion loss, DC power consumption, physical area, or implementation complexity.

Class C architectures follow a different bandwidth strategy by using lattice or all-pass synthesis to obtain relatively stable phase behavior over frequency. In the present dataset, Avci et al. (2019) demonstrated a symmetric-lattice phase shifter over 7.5–13 GHz, whereas Taş and Kaçar (2025) investigated an LC symmetric-lattice implementation over 4.5–5.5 GHz. These architectures can support relatively flat phase characteristics across the operating band. Nevertheless, their RF efficiency remains dependent on passive-component quality factors, switch loss, impedance matching, and component tolerances. Consequently, improved phase flatness does not necessarily imply lower insertion loss.

4.4. Qualitative Synthesis: Architecture Selection by Constraint

The cross-comparison of the 30 reviewed DPS designs does not support the existence of a universally superior topology. Instead, the results indicate that each architectural class becomes more or less suitable depending on the dominant constraint of the target application.

For high-power and low-complexity applications, passive Class A STPS architectures remain attractive because of their structural simplicity, high linearity, and low static power consumption in the RF path. These properties are particularly relevant to radar and satellite front ends, although insertion loss and physical area may become restrictive as bit count and bandwidth increase.

Class C lattice/all-pass architectures are more suitable when phase flatness over frequency is prioritized. Their application potential is strongest in broadband microwave front ends and moderate-frequency phased arrays, where passive-component quality factors and switching losses remain manageable.

When very high phase accuracy is the main objective, Class B VSPS/VMPS structures appear particularly attractive, especially when combined with digital calibration or precision weighting techniques, as demonstrated by Tu et al. (2025). In such cases, the observed performance advantage arises not only from the vector-sum principle itself, but also from the optimization framework used to suppress implementation error.

For sub-THz operation, the dataset suggests a change in architectural suitability. As frequency increases beyond 100 GHz, parasitic sensitivity and implementation fragility increasingly limit the practicality of conventional vector-sum approaches. Under these conditions, delay-based Class D solutions such as Uchino et al. (2025) appear more consistent with the physical constraints of the frequency range.

For fully integrated mmWave and sub-THz systems, several Class B implementations realized in advanced CMOS and FD-SOI technologies provide practical compromises among area, resolution, frequency capability, and phase accuracy. Minnella et al. (2025) demonstrated a compact 7-bit phase shifter in 28 nm FD-SOI CMOS, whereas Cho et al. (2025) reported two 8-bit vector-sum implementations in 28 nm CMOS for operation around 140 GHz. Tu et al. (2025) further showed that high phase accuracy can be achieved in 90 nm CMOS through digitally controlled current weighting. Although these designs do not dominate every performance metric, they illustrate the integration and calibration advantages of vector-based architectures.

Overall, the comparison shows that DPS evaluation should go beyond single-metric interpretation. Wide bandwidth does not necessarily imply an optimal overall design, low Pdc does not always guarantee system-level efficiency, and resolution alone does not ensure high accuracy. A more meaningful comparison emerges only when topology, technology node, calibration approach, and operating frequency are evaluated together.

To provide a concise design-oriented synthesis of these findings, Table 2 summarizes the principal strengths, limitations, and representative application domains associated with each architectural class. The table is intended to complement the detailed quantitative comparison in Table 1 by translating the observed architecture-level trade-offs into practical topology-selection guidance.

Table 1. Main characteristics, validation levels, and reported performance metrics of the reviewed digital phase-shifter designs

Ref	C	Subclass	Y	Band (GHz)	Bit / LSB	Topology	T	Switch/Element	IL / Gain	RMS φ err	RMS amp err	Pdc	Area
Xiong et al., 2020 [M]	B	VSPS (freq-reconfigurable)	2019	24–30 / 35–41	5b / 11.25°	Freq-reconf. active VSPS	90 nm CMOS	I/Q gen + VGA	Gain −5…−4.5 / −7…−5.9 dB	<4° / <5.1°	<0.6 / <0.35 dB	17.6 mW	0.34 mm²
Hamidi et al., 2019 [M]	D	Planar discrete PS (microstrip + hybrid)	2019	2.9–3.1	2b / 45°	Microstrip PS + 90° hybrid	Rogers 4350B	Passive transmission line	IL ~3.2 dB	max ~3.62° (Not RMS)	NR	0	NR
Luo et al., 2019 [M]	B	VSPS (active, QAF-based)	2019	6–18	6b / 5.625°	Active VSPS (QAF-based)	0.13 µm SiGe BiCMOS	main DAC(4b)+cal DAC(3b)	Gain 0.95→−1.85 dB	<4.36°	<1.04 dB	74.4 mW	1.8×1.3 mm²
Anjos et al., 2020 [M]	A	APN-based STPS (SP4T path select)	2019	14–50	2b / 45°	APN-based STPS + SP4T	0.25 µm SiGe:C BiCMOS	SP4T + 4×APN	IL 7.4±0.26 (28GHz); 10±0.22 (39 GHz)	<4°; <6°	<0.27 / <0.33 dB	0	0.48 mm²
Avci et al., 2019 [M]	C	Lattice / all-pass (symmetric lattice)	2019	7.5–13	3b / 45°	Symmetric lattice DPS	0.18 µm CMOS	NMOS + L/C	Loss ≤3.2 dB	4.9°	NR	NR	NR
Chiu et al., 2021 [M]	A	GaN STPS (high power)	2021	8–12	5b / 11.25°	GaN STPS	0.25 µm GaN HEMT-on-SiC	GaN switch	IL 11.8±3.45 dB	<6.23°	<1.15 dB	0	2×3 mm²
Wu et al., 2021 [M]	B	Passive vector-sum	2021	21.5–25	7b / 2.8125°	Passive VSPS	65 nm CMOS	Atten + DPDT + hybrid	Peak gain ~−14.3 dB	<2.1°	<1.2 dB	0	880×500 µm chip
Li et al., 2022 [M]	A	GaAs pHEMT STPS + compensation cell	2022	2.4–4.0	7b / 2.8° (+1.4° comp)	GaAs STPS	0.5 µm GaAs pHEMT	FET switch	Avg IL 4.5–4.9 dB	<3.1°; <1.5° (2.8–3.7)	<0.34 dB	NR	2.1×2.55; core 1.6×2.2 mm²
Lin and Tsai, 2022 [M]	A	CMOS STPS (HP/LP/T-type)	2022	32–41	5b / 11.25°	STPS HP/LP (T-type)	65 nm CMOS	MOS (body-floating)	IL 10.5–13.5 dB	2.4–6.2°	0.48–0.66 dB	NR	0.7×0.37 mm²
Zeng et al., 2023	A	GaAs pHEMT STPS (hybrid cells)	2023	12–18	6b / 5.625°	GaAs STPS	0.15 µm GaAs pHEMT	pHEMT switch	Avg IL 6.5–6.9 dB	RMS <2.8°	NR	NR	3.1×1 mm²
Song et al., 2023 [M]	A	Switched-filter STPS (GaN)	2023	37–40	6b / 5.625°	Switched-filter STPS	150 nm GaN HEMT	GaN switch	Min IL ~5 dB	<5.36°	RMS gain err 1.69–3.21 dB	0	2.82×1.19 mm²
Shangguan et al., 2024 [M]	B	Vector-modulated active PS	2024	8–18	6b / ~5.6°	Active vector-modulated	0.18 µm SiGe BiCMOS	Current array VM	Gain −0.5…1.8 dB	RMS <2°	RMS <0.5 dB	~65.3 mW	NR
Zhan et al., 2024 [M]	A	GaAs pHEMT STPS/MMIC	2024	2.5–3.3	6b / 5.625°	GaAs pHEMT multibit	0.5 µm GaAs pHEMT	pHEMT switch + driver	IL <4.3 dB	RMS <1.43°	ΔA <0.52 dB	NR	2.45×1.08 mm²
Taş and Kaçar, 2025 [S]	C	Lattice / all-pass (symmetric lattice)	2025	4.5–5.5	3b / 45°	LC symmetric lattice (all-pass)	ADS sim	Switched-C	RMS IL max 1.77 dB	RMS max 6.81°	NR	NR	NR
Minnella et al., 2025 [M]	B	VMPS/Vector-modulator	2025	37.5–40.5	7b / 2.8125°	VMPS (vector mod.)	28 nm FD-SOI CMOS	Gilbert-cell VM	Max IL 3.7 dB	2.7–4.7°	0.3–0.5 dB	13 mW	0.33 mm²
Lin and Lin, 2025 [SYS]	D	System/COTS (application-level)	2025	3.5–6.0	4b / 22.5°	COTS PS (system)	—	MAPS-010145	Avg IL ~5 dB	NR	NR	NR	NR
Ghorbani, 2025 [EB]	D	Enabling block: RF switch (not phase shifter)	2025	~2.05	—	PIN-diode RF switch + impedance transformer	PCB (RO4534)	BAR64-03V (N=1/2/4 parallel)	IL <1.2/<1.0/<0.7 dB	—	—	—	—
Ghorbani, 2025 [EB]	A	Switched-line STPS (PCB)	2025	1.9–2.2	3b / 45°	Switched-line PS	PCB	4 PIN parallel RF switch	Total IL 4.2 dB	NR	NR	NR	NR
Ghorbani, 2025 [EB]	A	Loaded-line STPS (PCB)	2025	1.8–2.5	1b / 45°	Loaded-line (stub ground control)	PCB	PIN diodes	Max IL 2.1 dB	NR	NR	NR	NR
Cho et al., 2025 [PL]	B	VSPS (Gilbert VGA)	2025	140–157	8b / 1.406°	VSPS – Gilbert-cell VGA	28 nm CMOS	Marchand+Lange + 13-bit DAC	Peak gain −9.5 dB	Max RMS 6°	Max RMS 2 dB	49 mW	NR
Cho et al., 2025 [PL]	B	VSPS (current-steering VGA)	2025	129–144	8b / 1.406°	VSPS – current-steering VGA	28 nm CMOS	Marchand+Lange + 13-bit DAC	Peak gain −5.1 dB	Max RMS 4.8°	Max RMS 1.3 dB	29 mW	NR

C= class, Y= year, T= technology STPS= switch-type phase shifter, VSPS= vector-sum phase shifter, VMPS= vector-modulator phase shifter, IL= insertion loss, RMS= root mean square, Pdc= DC power consumption, NR= not reported, COTS= commercial off-the-shelf, NEMS= nanoelectromechanical systems. Validation level: [M], measured, [PL], post-layout/EM simulation, [S], schematic-level simulation, [NM], numerical modeling, [SYS], system-level demonstration, [EB], enabling-block study.

Table 1. Main characteristics, validation levels, and reported performance metrics of the reviewed digital phase-shifter designs (continued)

Ref	C	Subclass	Y	Band (GHz)	Bit / LSB	Topology	T	Switch/Element	IL / Gain	RMS φ err	RMS amp err	Pdc	Area
Uchino et al., 2025 [M]	D	Delay-based (FFPS/PDPS fine resolution)	2025	150–160	fine 0.1° + coarse 22.5°	FFPS + NU-PDPS	65 nm CMOS	Varactor + MOS net	IL 2.5 dB	0.68°	1.19 dB	5 mW	0.06 mm^2
Jiang et al., 2025 [M]	B	VSPS (active, state selection)	2025	20–30	64-state	Active VSPS (QSG+VM+VGA)	0.18 µm SiGe BiCMOS	Tail-current controlled	Gain var. −1.2…0.1 dB	<2°	(Not RMS) −1.2…0.1 dB	19.5 mW @2.5 V	0.4 mm^2 (core 0.165)
Shen et al., 2025 [M]	A	STPS (SiGe, coupler-based 180°)	2025	90–100	6b / 5.625°	STPS; 180° coupler–LP	0.13 µm SiGe BiCMOS	Switch transistors	12–15.5 dB	<2.3°	<0.9 dB	NR	0.39 mm^2
Tu et al., 2025 [M]	B	VSPS (active, IDAC-weighted)	2025	27–31	7b / 2.8125°	Active VSPS (LC QAF + adder)	TSMC 90 nm CMOS	2×8-bit IDAC + adder	Avg gain 0.13–1.36 dB	0.18–0.21°	0.68–0.9 dB	10 mW	0.63 mm^2
Khazaei et al., 2025 [M]	A	Switched-line (Schiffman/ microstrip, PIN)	2025	2.2–3.322 (center frequency)	4b / 22.5°	Modified Schiffman	RO4003 microstrip	PIN SMP1321-040LF	Avg IL <4 dB	RMS <8.1°	NR	NR	NR
Sindhuja et al., 2025 [NM]	D	NEMS DNTL (discrete state)	2025		3b (45/90/180)	DNTL NEMS TL PS	Si/CPW + HfO_2	33 NEMS membran	Avg IL ~0.6 dB	±2° (Not RMS)	NR	~0	NR
Kilinc et al., 2026 [S]	A	STPS with active inductors (integrated)	2026	2.2–3.6	5b / 11.25°	STPS + active inductors	0.18 µm CMOS	MOS + gyrator-C AI	Avg IL ~14 dB	RMS <3.3°	NR	NR	0.17 mm^2
Lee et al., 2026 [M]	B	VSPS/Vector-sum (current-steering)	2026	10.7–12.7	6b / 5.625°	Current-steering VSPS	130 nm BiCMOS	RF-cell array	Gain −2.17–4.55 dB	≤2.5°	0.3–0.5 dB	15.8 mW	1.75×1.1 1 mm^2
Wei et al., 2026 [M]	B	VSPS + reconfigurable PPF	2026	2–18	6b / 5.625°	VSPS + reconfigurable PPF	0.13 µm SiGe BiCMOS	Varactor + IDAC	Gain 1.5–3.2 dB	<1.5°	<1.2 dB	105 mW	1240×860 µm^2

C= class, Y= year, T= technology STPS= switch-type phase shifter, VSPS= vector-sum phase shifter, VMPS= vector-modulator phase shifter, IL= insertion loss, RMS= root mean square, Pdc= DC power consumption, NR= not reported, COTS= commercial off-the-shelf, NEMS= nanoelectromechanical systems. Validation level: [M], measured, [PL], post-layout/EM simulation, [S], schematic-level simulation, [NM], numerical modeling, [SYS], system-level demonstration, [EB], enabling-block study.

Table 2. Architecture-level design trade-offs and representative application domains

Class	Architecture	Main strengths	Main limitations	Most suitable application domains
A	STPS	High linearity; simple control; zero or low static RF-path power in passive realizations	Insertion loss and area increase with bit count; parasitic sensitivity at mmWave frequencies	High-power radar, satellite front ends, low-complexity phased arrays
B	VSPS/VMPS	High resolution; calibration flexibility; active gain compensation	DC power consumption; I/Q mismatch; gain–phase coupling; calibration complexity	High-accuracy beamforming, active antenna arrays, mmWave and 6G transceivers
C	Lattice/all-pass	Wideband phase flatness; stable phase response; good matching potential	Passive loss; component-Q sensitivity; limited scalability at very high frequencies	Broadband microwave systems, phase-flat front ends, moderate-frequency arrays
D	Special/other	Fine delay-based resolution; NEMS low-power potential; system-specific flexibility	Heterogeneous maturity; limited comparability; integration and scalability challenges	Sub-THz systems, RIS, specialized radar, system/COTS demonstrations

4.5. Limitations

The conclusions presented in this review should be interpreted in light of several limitations. First, the reviewed studies span different operating frequencies, technologies, and validation levels, making perfectly fair comparison impossible. Second, several publications do not report RMS amplitude error, large-signal linearity, or complete calibration procedures. Third, some recent studies are available only as simulation or post-layout results rather than measured IC implementations. Consequently, the reported trends should be interpreted as evidence-supported observations rather than absolute rankings.

4.6. Future Research Directions

Future research on digital phase shifters is expected to transition from isolated circuit optimization toward system-integrated, reconfigurable, and calibration-aware design strategies. The application of artificial intelligence (AI) and machine learning (ML) techniques to phase-state optimization, calibration, process–voltage–temperature (PVT) compensation, and the prediction of parasitic-induced performance degradation represents a

promising research direction. In high-resolution vector-sum systems, where gain–phase coupling and large state spaces make conventional manual tuning increasingly challenging, data-driven optimization techniques may provide significant benefits.

A second research direction is the development of digital phase shifters for large-scale 6G beamforming systems and reconfigurable intelligent surfaces (RIS). Such applications require compact implementations, scalable control architectures, tolerance to device and process variations, and very low per-element power consumption. Low-complexity calibration techniques, distributed control strategies, and passive or hybrid phase-shifting architectures are therefore expected to become increasingly important for large-scale array implementations.

Operation at sub-THz frequencies remains a major design challenge because passive loss, device parasitics, layout sensitivity, and power-efficiency limitations become increasingly severe as the operating frequency approaches and exceeds 100 GHz. In this frequency range, delay-based, hybrid vector-delay, and digitally assisted architectures may provide viable alternatives to conventional phase-shifter topologies. Future studies should therefore evaluate not only nominal phase resolution but also the number of effectively usable phase states under process, voltage, temperature, device mismatch, packaging, and interconnect variations.

Finally, more standardized reporting practices should be encouraged to improve the reproducibility and comparability of future digital phase-shifter research. In particular, studies should consistently report RMS phase error, RMS amplitude error, insertion loss or gain, large-signal linearity metrics, calibration techniques, validation level, and measurement conditions. Such standardized reporting would enable more reliable cross-study comparisons and provide a stronger basis for evaluating the suitability of different architectures for emerging 6G, RIS, mmWave, and sub-THz applications.

5. Conclusion

This review systematically examined 27 papers covering a total of 30 digital phase-shifter designs, including switch-type phase shifters (STPS), vector-sum/vector-modulator-based architectures (VSPS/VMPS), lattice/all-pass-network-based solutions, and special categories such as delay-based fine-resolution and NEMS-related approaches. Because the literature exhibits substantial heterogeneity in topology, technology platform, operating frequency, and validation depth, the comparison was conducted using a multi-metric and evidence-aware framework. In this framework, measured IC/MMIC demonstrations were given primary emphasis as the strongest evidence of practical behavior, whereas post-layout or schematic-level studies, system/COTS demonstrations, and enabling-block works were treated as supporting evidence for architectural interpretation and trend analysis.

Several consistent observations emerged from the cross-comparison. First, practical phase accuracy depends more strongly on state consistency over frequency, parasitic-aware implementation, and the availability of calibration or compensation mechanisms than on nominal bit resolution alone. Accordingly, bit count should not be treated as a sufficient predictor of real accuracy. Second, STPS architectures remain attractive for applications requiring low complexity and little or no DC power in the RF path; however, as bandwidth and resolution targets increase, the trade-off among insertion loss, area, and achievable accuracy generally becomes more severe. Third, vector-based architectures offer a flexible route to broadband phase synthesis and, in active implementations, can partially compensate RF loss through gain. These benefits, however, are typically accompanied by increased sensitivity to I/Q imbalance, weighting mismatch, calibration complexity, and non-negligible DC power consumption. Fourth, lattice- and all-pass-network-based designs remain relevant when phase flatness across frequency is the dominant requirement, although this benefit is often achieved at the cost of increasing passive loss as frequency rises. Finally, delay-based approaches appear especially promising for sub-THz operation, where parasitic effects and implementation nonidealities increasingly limit the robustness of more conventional solutions.

The review also highlights several persistent reporting gaps in the literature. Although RMS phase error is reported more frequently than in earlier studies, RMS amplitude error, large-signal linearity metrics, and explicit descriptions of calibration or state-selection procedures are still not provided consistently. This limits the ability to compare designs fairly and to infer array-level consequences such as beam-pattern degradation, gain variation, and high-power behavior directly from published results. Future work would therefore benefit from more standardized reporting practices, including routine disclosure of large-signal metrics such as P1dB and IIP3, full-band and full-state evaluation of RMS phase and RMS amplitude errors, and clearer descriptions of calibration-aware measurement and optimization procedures.

Overall, the reviewed evidence does not support the existence of a universally optimal digital phase-shifter topology. Instead, the most suitable architecture depends on the dominant application constraint, whether it is ultra-high accuracy, wide bandwidth, low power, compact area, or scalability toward mmWave and sub-THz systems. Future scalable solutions will likely rely increasingly on reconfigurable or hybrid architectures, calibration-aware design strategies, and maximizing the number of effectively usable states under parasitic effects and process-voltage-temperature (PVT) variations. The taxonomy, evidence-aware methodology, and cross-comparison framework presented in this review are intended to support more informed topology selection while also improving reproducibility, transparency, and

comparability in future digital phase-shifter research.

Author Contributions

The percentages of the authors' contributions are presented below. All authors reviewed and approved the final version of the manuscript.

	S.T.	F.K.
C	60	40
D	60	40
S	30	70
DCP	70	30
DAI	70	30
L	70	30
W	75	25
CR	40	60
SR	70	30
PM	60	40

C=Concept, D= design, S= supervision, DCP= data collection and/or processing, DAI= data analysis and/or interpretation, L= literature search, W= writing, CR= critical review, SR= submission and revision, PM= project management.

Conflict of Interest

The authors declared that there is no conflict of interest.

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