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Reconfigurable Field Programmable Analog Array–Based Filtering of Electrocardiogram Signals

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WHAT IS ALREADY KNOWN ON THIS TOPIC?

- *Surface electrocardiogram (ECG) signals are easily affected by baseline drift, motion, muscle activity, poor electrode contact, power-line interference, and equipment noise.*
- *Noise can obscure important ECG waveform components, including the QRS complex, so effective filtering is necessary for reliable signal interpretation.*
- *Electrocardiogram noise reduction can be performed with analog filters, digital finite impulse response/infinite impulse response (FIR/IIR) filters, wavelet methods, and adaptive algorithms, but implementation complexity can limit hardware flexibility.*

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ABSTRACT

This paper aimed to develop a reconfigurable, adaptable hardware platform based on a field programmable analog array (FPAA) for filtering electrocardiogram (ECG) signals. The system enables the redesign of analog filtering parameters to suit signal shape or medical needs. The ECG signals are acquired using Einthoven's three-lead configuration and converted into raw digital data with the BIOPAC MP35 device (BIOPAC Systems, Inc., Goleta, CA, USA). To convert the digital raw ECG signal to an analog signal, a field-programmable gate array (FPGA) device is employed, enabling simultaneous operation with an R-2R ladder digital-to-analog converter. The FPGA converts the raw digital ECG signal into an analog signal. Consequently, integration of FPAA and FPGA devices forms an adaptable biosignal acquisition and filtering platform. Surface ECG signal acquisition is inherently vulnerable to noise due to the microvolt-level amplitude and low-frequency spectrum (0.5–100 Hz) of cardiac biopotentials. Major interferences arise from both physiological sources—such as respiratory baseline wandering and muscle activity—and environmental factors, including 50/60 Hz power-line hum, equipment noise, and poor electrode contact. Left unfiltered, these disturbances distort essential waveform components (P wave, QRS complex, and T wave), compromising signal integrity and increasing the risk of clinical misdiagnosis. The FPAA platform combines software, hardware, and algorithms into a single compact unit. Traditionally, ECG signal filtering requires an analog stage for amplification and filtering. Recently, FPAA has emerged as a flexible, rapid-prototyping platform for developing complex analog acquisition and filtering systems for ECG monitoring. This study introduces a method for filtering ECG signals using the FPAA device, which is based on Anadigm filter technology. The filter types (low-pass [LP], high-pass [HP], and notch filter [NF]) for ECG signals are configured using AnadigmDesigner2 on a computer and programmed into the hardware. The fully filtered FPAA output achieved an ensemble-based signal-to-noise ratio of 24.48 dB, corresponding to a 7.82 dB improvement relative to the raw ECG. The device's filtering capability was evaluated using an FPAA board and compared with Biopac simulation results. The experimental results demonstrate the functional operation of the proposed FPAA-based filtering platform.

***Index Terms*—**AN231E04, AnadigmDesigner2, BIOPAC, electrocardiogram (ECG), field programmable analog array (FPAA)

I. INTRODUCTION

Regular examination is crucial for early diagnosis [1]. Analog integrated circuit technology is always needed to acquire raw patient data. field programmable analog array (FPAA) technology allows easy construction of analog systems for filtering raw electrocardiogram (ECG) signals. After processing, the signal can be analyzed using AnadigmDesigner2 software.

Field programmable analog array hardware dynamically reconfigures its filter topologies and parameters to support additional data sampling requirements. Field programmable analog array ICs allow changing the circuit's configuration and reprogramming it during operation, so it is not necessary to shut down and reprogram the device repeatedly, as in the cases of previous microprocessor circuits. Given the ECG signal characteristics (low-amplitude differential voltage, elevated noise, and low-frequency range), the FPAA device is well-suited for filtering raw data [2].

The data acquisition platform is based on a Biopac MP35 device, which collects analog raw data and digitizes it. The field programmable gate array (FPGA) accelerates digital data by a factor of

WHAT THIS STUDY ADDS TO THIS TOPIC?

- *The study implements a reconfigurable ECG-filtering platform that combines BIOPAC MP35 acquisition, field programmable gate array–based 1000-fold time scaling, a 16-bit R-2R digital-to-analog converter, and an AN231E04 field-programmable analog array (FPAA).*
- *The 1000-fold time-scale transformation shifts the required very-low-frequency ECG filter cutoff into a range that a single FPAA board can realize without redesigning the analog filtering hardware.*
- *The fully filtered FPAA output increased the ensemble-based signal-to-noise ratio from 16.66 dB to 24.48 dB (+7.82 dB), although R-peak attenuation remained a limitation.*
- *Experimental results confirm the functional operation of the high-pass, low-pass, and notch filter stages and show waveform trends consistent with simulation outputs.*

1000, then converts it back to analog using an R-2R ladder digital-to-analog converter (DAC). The raw data are upsampled by a factor of 1000 primarily to shift the cutoff frequency of the applied filters to higher frequencies. After that, the accelerated analog data are applied as an input signal to the FPAA.

- Surface ECG recordings are highly sensitive to noise, including baseline drift, motion artifacts, poor electrode contact, muscle activity, power-line interference, and equipment-related disturbances.
- Electrocardiogram noise removal is essential for reliable signal interpretation and accurate detection of important waveform components such as the QRS complex.
- Several ECG filtering methods have been reported, including analog filters, digital finite impulse response (FIR)/infinite impulse response filters, wavelet-based methods, and neural-network-based adaptive filtering; however, some digital approaches may require high-order filter structures and increased design complexity.
- This study presents a reconfigurable FPAA-based hardware approach for ECG noise removal using filter structures designed in AnadigmDesigner2.
- The proposed system combines BIOPAC MP35 ECG acquisition, FPGA-based signal acceleration, digital-to-analog conversion, and FPAA-based analog filtering in a hybrid analog–digital platform.
- The experimental results demonstrate the functional feasibility of the FPAA-based platform, showing visual waveform trends consistent with reference outputs from BIOPAC and AnadigmDesigner2.

This paper is organized as follows: Section II reviews the relevant literature and briefly summarizes prior studies on this subject, summarizes the fundamentals of analog processing of the ECG signal, which is usually required for its acquisition, and also reviews the convenience of FPAA for ECG signal filtering and shows the required filter types implemented within the device. The simulated ECG signal features these filter configurations. Section III summarizes the overall architecture of that reconfigurable structure and the implementation of ECG signal acquisition, including measurement results. Section IV discusses the experimental findings. Finally, Section V presents the conclusions and directions for future work.

II. GENERAL OVERVIEW

A. Literature Review

Electrocardiogram acquisition is highly susceptible to interference because cardiac biopotentials have relatively low amplitudes and occupy a low-frequency range. Typical disturbances include baseline wander, electrode-motion artifacts, electromyographic interference, poor electrode contact, power-line interference, and instrumentation noise. Since these disturbances may overlap with diagnostically relevant ECG components, an effective denoising method should suppress unwanted components while preserving the morphology of the P wave, QRS complex, and T wave. This requirement is particularly important for low-amplitude components such as the P wave, whose detection becomes more difficult at low signal-to-noise ratios (SNRs) [3]. Fig. 1 presents an example of a noise-contaminated ECG signal. A schematic representation of the normal heart rhythm is shown in Fig. 2 [4]. The P wave represents atrial depolarization, the QRS complex corresponds to ventricular depolarization, and the T wave represents ventricular repolarization [3].

Conventional digital filtering remains widely used because of its deterministic response and straightforward implementation. Early studies demonstrated that FIR filters, combined with oversampling, can effectively filter ECG signals while preserving waveform characteristics [5]. Wavelet-based approaches have also been investigated because of the non-stationary nature of ECG signals. For example, the undecimated wavelet transform has been applied to ECG noise reduction and QRS detection [6]. Adaptive methods offer additional flexibility; Poungponsri and Yu proposed a neural network-based approach for ECG noise reduction [7].

More recent research has revisited conventional filtering using modern implementation platforms. Basu and Mamud investigated the effects of Butterworth filter order and cutoff frequency on ECG noise reduction and demonstrated that filter parameters strongly influence the balance between noise suppression and useful-signal preservation [8]. Bui and Byun compared FIR and IIR filters at different sampling frequencies using both recorded data and real-time ECG

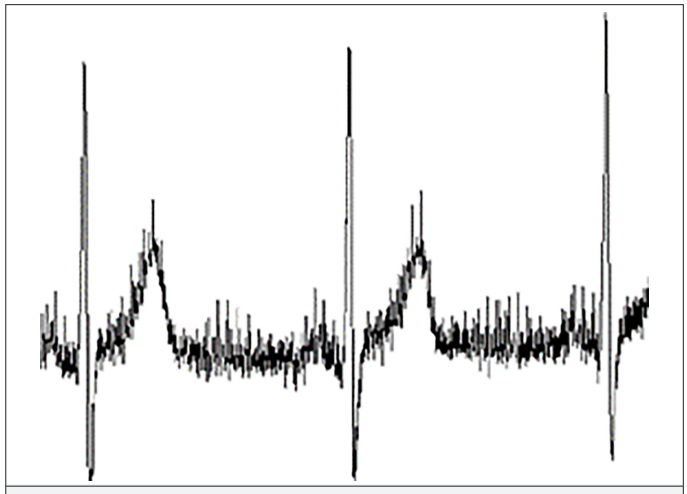


Fig. 1. Raw ECG signal. ECG, electrocardiogram.

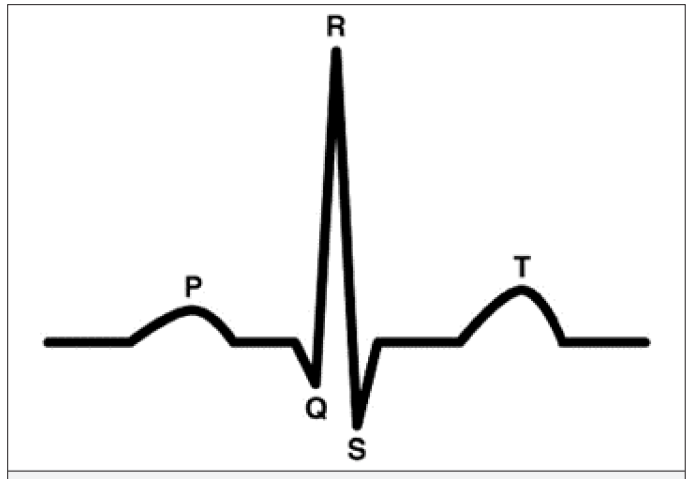


Fig. 2. Schematic representation of normal cardiac rhythm.

measurements, demonstrating that sampling frequency and filter structure affect signal quality and computational requirements [9]. These studies indicate that conventional FIR and IIR filters remain effective when their parameters are appropriately selected for the required ECG bandwidth and implementation platform.

Recent ECG research has also shifted toward adaptive algorithms and hardware-accelerated processing. Li et al. proposed an improved variational mode decomposition (VMD) method in 2022 that combines empirical mode decomposition (EMD) with adaptive particle swarm optimization. Their method was evaluated onMassachusetts Institute of Technology–Beth Israel Hospital (MIT-BIH) data and experimentally recorded ECG signals, and improvements in SNR, mean-square error, and correlation coefficient were reported compared with conventional EMD and VMD methods [10]. In the same year, Dhas and Suchetha implemented a non-causal adaptive filter for fetal ECG extraction on a Virtex-7 FPGA (Xilinx, Inc., San Jose, CA, USA), demonstrating the suitability of programmable digital hardware for computationally intensive ECG processing [11].

Field-programmable gate array-based implementations have become increasingly important for real-time biomedical signal processing. Zhu et al. developed a multichannel ECG acquisition system in which the analog front end performs amplification and filtering. At the same time, the FPGA manages analog-to-digital conversion, real-time visualization, and data storage [12]. More recently, Saha and Mandal proposed an FPGA-based composite ECG denoising filter in 2026. Their architecture combines an elliptic high-pass (HP) IIR filter, a moving-average FIR filter, and an elliptic band-stop IIR filter. The implementation was evaluated using 376 ECG recordings and achieved 2.61% FPGA resource utilization, demonstrating the feasibility of resource-efficient digital ECG denoising [13].

In parallel with digital processing, substantial research has focused on low-power analog front ends and portable ECG acquisition systems. Kumngern et al. developed a 0.5 V fifth-order Butterworth low-pass (LP) filter for ECG applications, reporting a simulated bandwidth of 250 Hz and power consumption of 34.65 nW [14]. Bano et al. proposed a fourth-order analog LP filter for portable ECG acquisition [15]. Watcharapongvinit et al. developed a two-electrode ground-free ECG analog front end with common-mode interference suppression, achieving 6.55 μW power consumption and 1.67 μVrms input-referred noise over a 1–100 Hz bandwidth [16]. More recently, Luiz et al. presented a portable ECG/EMG acquisition platform in 2025 with up to eight channels, 24-bit resolution, configurable sampling rates of 1–4 kHz, bluetooth communication, and approximately 22.3 hours of battery operation [17]. These studies demonstrate the current emphasis on low-power operation, portability, signal integrity, and efficient hardware implementation.

To provide a structured comparison of existing ECG-processing systems, selected studies are summarized in Table I by implementation method, reconfigurability, and main outcome. The comparison includes digital filtering approaches, FPGA-based systems, low-power analog front ends, portable acquisition platforms, and reconfigurable FPAA-based implementations.

As summarized in Table I, recent studies primarily address digital denoising, FPGA-based processing, low-power analog front-ends, or portable ECG acquisition. Field-programmable gate array implementations provide flexible digital processing, whereas dedicated analog circuits generally provide low-power operation but have fixed circuit structures. Field programmable analog array technology offers an alternative approach by enabling analog filtering functions and parameters to be reconfigured without redesigning the physical circuit.

B. Field Programmable Analog Array–Based ECG Signal Processing

Field programmable analog arrays enable configurable analog functions to be implemented using programmable analog blocks and interconnections. Chan et al. demonstrated an FPAA-based bioelectric front end capable of conditioning both ECG and EMG signals using the same programmable hardware [18]. Morales et al. later combined FPAA-based analog conditioning with FPGA-based digital processing in a reconfigurable ECG acquisition system. Their platform enabled modification of parameters such as gain and bandwidth and supported subsequent FIR, wavelet, and QRS-related processing [2]. Related work by Morales et al. also demonstrated an FPGA–FPAA ECG acquisition architecture with wavelet-based digital processing [19].

Researchers subsequently extended FPAA-based ECG systems to embedded and intelligent applications. Tran et al. employed an FPAA for ECG acquisition and preprocessing, using cascaded HP, LP, and NFs before neuro-fuzzy classification [1]. Kay and Iaione developed

TABLE I. COMPARISON OF ECG FILTERING AND ACQUISITION SYSTEMS WITH THE PROPOSED PLATFORM

Study	Method/Platform	Reconfigurable	Main Outcome
Morales et al. [2], 2011	FPAA + FPGA	Yes	Reconfigurable ECG acquisition and processing
Kay and Iaione [20], 2015	FPAA + MCU	Yes	Wireless ECG acquisition and gain control
Bui and Byun [9], 2021	FIR/IIR filtering	Digital only	Real-time ECG filtering
Li et al. [10], 2022	Improved VMD	No	Improved ECG denoising and morphology preservation
Watcharapongvinit et al. [16], 2023	Low-power CMOS AFE	No	Low-noise and low-power ECG acquisition
Luiz et al. [17], 2025	Portable ECG/EMG platform	Partly	High-resolution wireless acquisition
Saha and Mandal [13], 2026	FPGA-based IIR-FIR-IIR	Digital only	Hardware-based ECG noise reduction
Proposed study	BIOPAC + FPGA + DAC + FPAA	Yes	Reconfigurable hardware-based ECG filtering

AFE, analog front end; CMOS, complementary metal-oxide-semiconductor; DAC, digital-to-analog converter; ECG, electrocardiogram; EMG, electromyography; FIR, finite impulse response; FPAA, field-programmable analog array; FPGA, field-programmable gate array; IIR, infinite impulse response; MCU, microcontroller unit; VMD, variational mode decomposition.

an AN221E04-based embedded ECG acquisition system and implemented analog amplification and filtering within the FPAA. At the same time, an android-based interface allowed users to reconfigure selected parameters [20]. These studies establish that FPAA-based ECG processing and the combined use of FPGA and FPAA devices are already present in the literature. Therefore, the contribution of the present study should not be attributed solely to the combination of these programmable technologies.

The research gap, instead, concerns the specific signal-processing architecture implemented in the present work. The ECG signal is first acquired and digitized using the BIOPAC MP35 platform. The recorded digital data are then time-scaled by a factor of 1000 using the FPGA and reconstructed in the analog domain through a 16-bit R-2R ladder DAC. The reconstructed signal is subsequently processed by an AN231E04 FPAA configured with HP, LP, and NF stages in AnadigmDesigner2.

The FPGA-based time-scale transformation represents an important engineering feature of the proposed architecture. Because the very-low-frequency HP cutoff required for ECG processing cannot be directly implemented with the single FPAA configuration used in this prototype, the ECG time scale is increased before analog reconstruction. This operation shifts the corresponding filter frequencies to a specific range. The signal is then reconstructed through the R-2R DAC and applied to the programmable analog filtering stage.

None of the studies reviewed in this work reported the specific BIOPAC MP35-FPGA time-scaling-R-2R DAC-FPAA processing sequence. Accordingly, the contribution of the proposed system is the system-level implementation and experimental validation of this hybrid analog–digital ECG filtering architecture, rather than the individual use of FPGA or FPAA technology. The architecture combines programmable digital time scaling with reconfigurable analog filtering, enabling the practical low-frequency limitation of the single FPAA board to be addressed without redesigning the analog filter hardware.

III. MATERIALS AND METHODS

Fig. 3 shows the system's block diagram. It summarizes the complete signal path. The system receives ECG signals from three electrodes directly connected to the Biopac device, whereas all electronic circuitry required to filter the ECG signal is built into the FPAA. (AN231E04, Anadigm Inc., Mesa, AZ, USA).

A. Ethical Considerations and Electrocardiogram Data Source

The raw ECG signals utilized to evaluate the FPAA-based noise removal architecture were collected exclusively from the primary author (self-experimentation) using non-invasive surface electrodes. As this study focuses strictly on the technical validation of reconfigurable hardware filtering and involves no external human participants, clinical trials, or diagnostic evaluations, formal ethics committee approval was not required.

B. Data Acquisition With BIOPAC MP35

The BIOPAC Student Lab (BSL) system has data-acquisition equipment with built-in amplifiers to record and process electrical signals

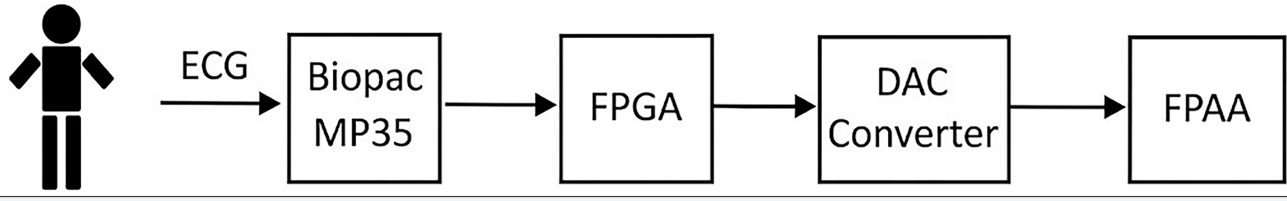


Fig. 3. System block diagram for acquiring and filtering ECG signals.

from the heart, muscles, nerves, and brain. It receives signals from electrodes or transducers, then digitizes the data and filters out noise. Electrical signals are very small—amplitude levels can drop to microvolts—so the Biopac equipment amplifies these ECG signals when it digitizes them [21]. Fig. 4 depicts the acquisition and electrode-placement configuration for the BIOPAC MP35 four-channel system, which integrates hardware and software for data collection [22-23].

In this article, two software technologies (BSL and AnadigmDesigner2) will be compared to filter the ECG signal from noise. The raw signal was filtered directly using the Biopac device, and then the same signal was also filtered with the FPAA card. Finally, the results were compared.

Note that, in the first step, the raw data are obtained by the Biopac device and then accelerated with an FPGA board. After that, the signal obtained from the FPGA device is converted with the D/A converter. Finally, the proposed ECG filtering system is used to purify the signal using the FPAA device.

C. AnadigmDesigner2

Fig. 5 shows the FPAA internal configuration in AnadigmDesigner2. The input signal "1" is the raw ECG signal measured and transferred to the digital environment by BIOPAC MP 35. The resulting signal was applied to the circuit input to eliminate noise. The signal "2" is the filtered electrical signal by BIOPAC MP 35.

The signal-processing pipeline utilizes configurable analog modules arranged in a three-stage cascade: (I) fourth order filter: NF(Fc = 50 kHz); (II) bilinear filter: DC blocking HP filter with LP filter (Fc = 42 Hz–150 kHz), G = 1; (III) biquadratic filter: LP filter (Fc = 8 kHz), G = 1.

The signals filtered by both Anadigm and Biopac are shown in Fig. 6. The green signal represents the raw input signal; the yellow signal represents the intermediate response after stages (I) and (II); the turquoise signal represents the fully filtered ECG by AnadigmDesigner2; and the purple signal represents the ECG filtered by Biopac.

Fig. 7 compares the ensemble-averaged raw ECG with the intermediate, fully filtered FPAA, and BIOPAC-filtered outputs, highlighting the changes in waveform morphology and R-peak amplitude.

D. Quantitative Noise and Signal-to-Noise Ratio Analysis

To quantitatively evaluate the noise-reduction performance of the proposed filtering architecture, an ensemble-based SNR analysis was performed. Each beat was aligned to its R peak and baseline-corrected before analysis. For each signal, the ensemble-average waveform was considered the repeatable ECG component, while the beat-to-ensemble deviations were considered residual variability and noise.

For K aligned ECG beats, the ensemble-average waveform was calculated as

$$\bar{x}[n] = \frac{1}{K}\sum_{k=1}^{K} x_k[n] \quad (1)$$

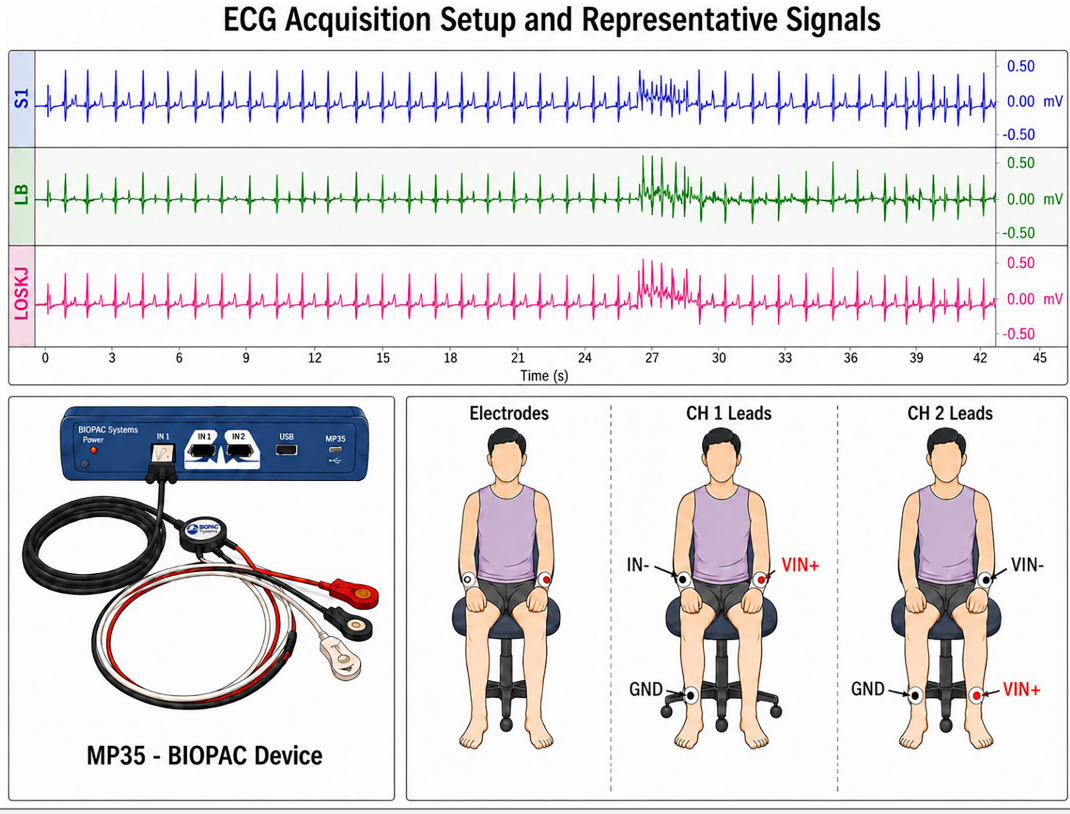


Fig. 4. ECG recording using BSL MP 35 bipolar leads. ECG, electrocardiogram; BSL, BIOPAC Student Lab.

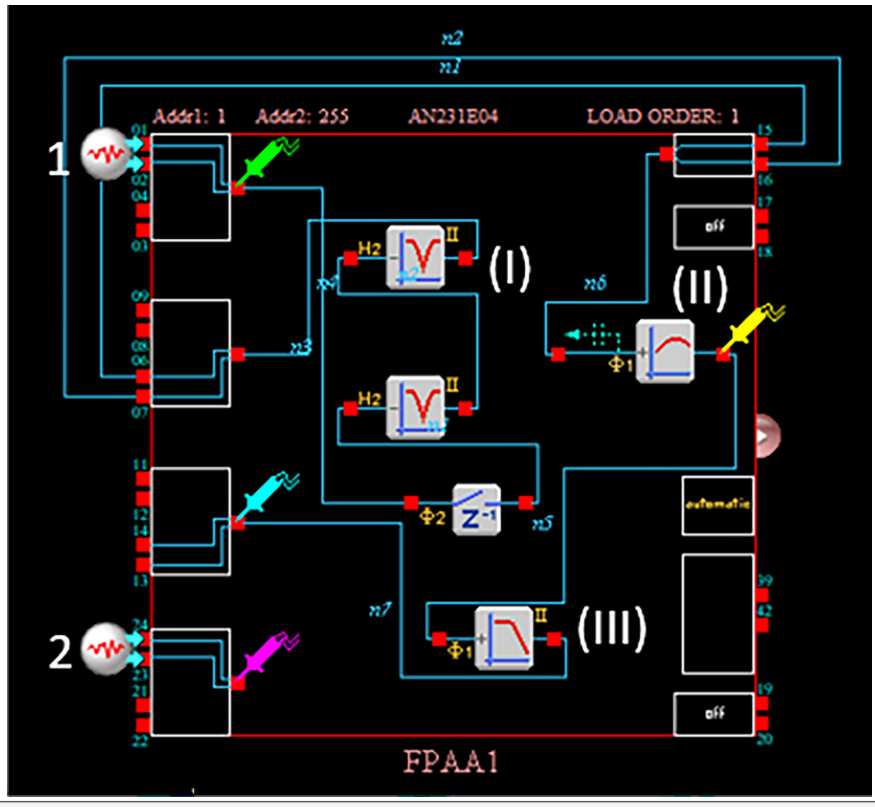


Fig. 5. Design of filter blocks using AnadigmDesigner2.

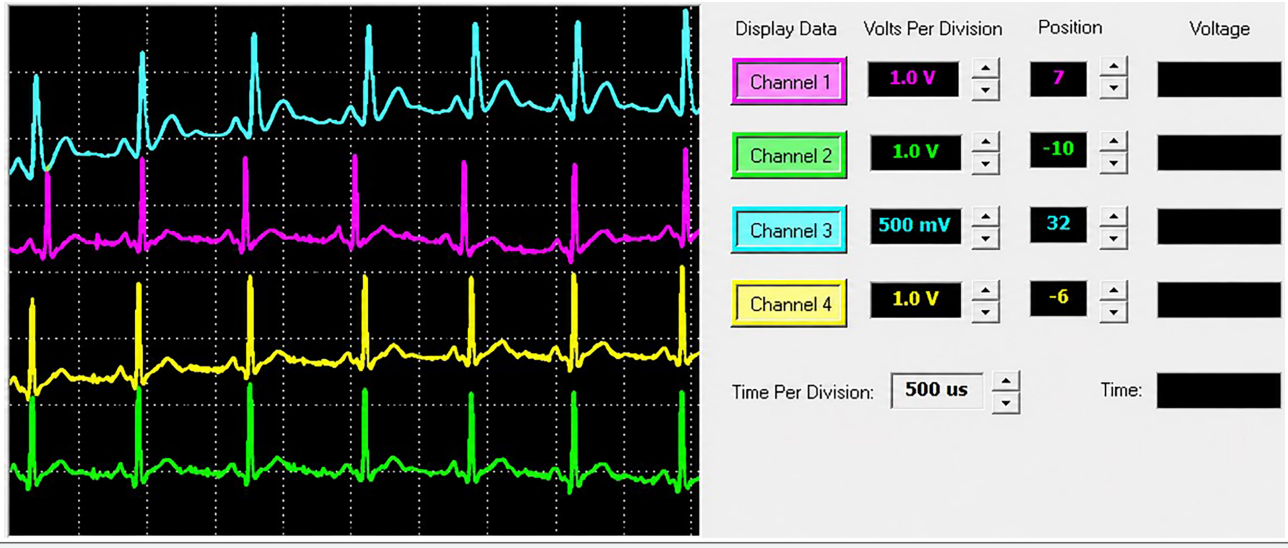


Fig. 6. ECG signal time domain response. ECG, electrocardiogram.

The residual component of each beat was then calculated as

$$e_k[n] = x_k[n] - \bar{x}[n] \tag{2}$$

The ensemble signal and residual-noise powers were calculated as

$$P_s = \frac{1}{N}\sum_{n=1}^{N}\bar{x}^2[n] \tag{3}$$

and

$$P_n = \frac{1}{KN}\sum_{k=1}^{K}\sum_{n=1}^{N}e_k{}^2[n] \tag{4}$$

The ensemble-based SNR was calculated as

$$SNR = 10\log_{10}\left(\frac{P_s}{P_n}\right) \tag{5}$$

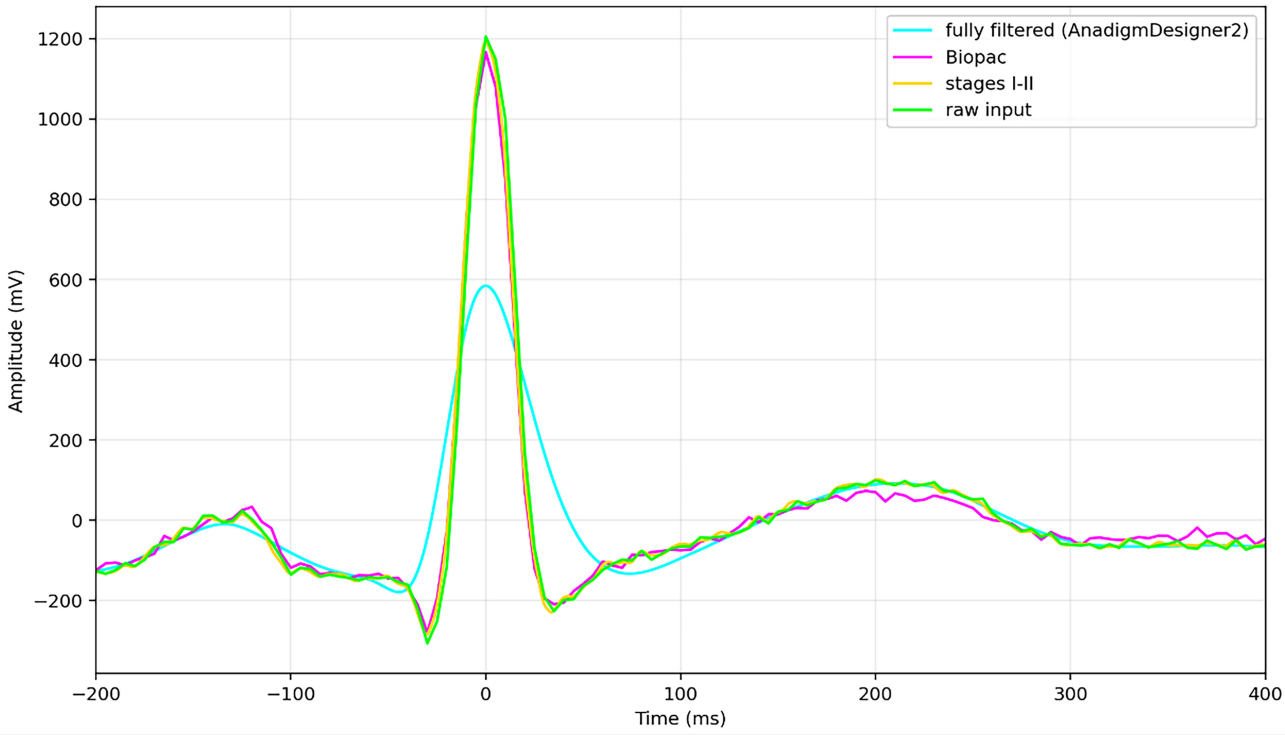


Fig. 7. Ensemble-averaged ECG waveforms for the raw input and filtered outputs. ECG, electrocardiogram.

Since an independently measured noise-free ECG reference was not available, the reported values are interpreted as ensemble-based SNR estimates rather than absolute physiological SNR values.

E. Hardware Implementation

The experimental setup verifies the operation of the complete FPGA–DAC–FPAA signal chain for real-time ECG filtering. Fig. 8 depicts the experimental hardware testbed configured to empirically validate the real-time performance of the proposed signal conditioning architecture.

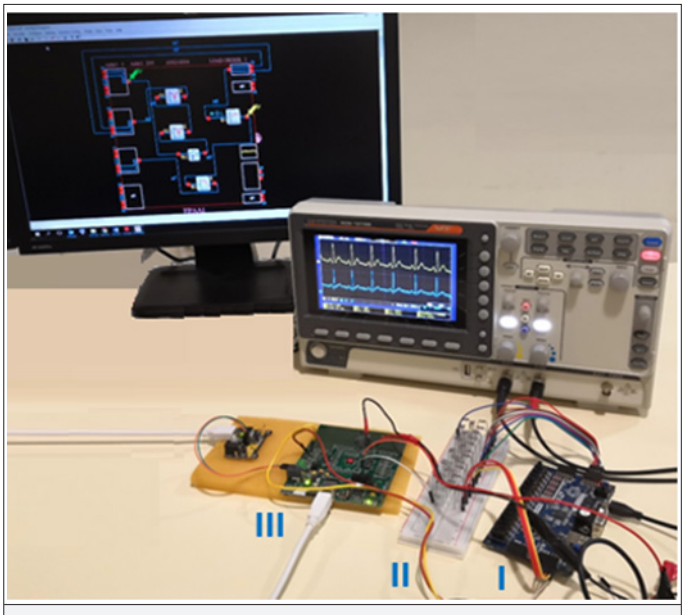


Fig. 8. Hardware implementation of ECG signal filtering. ECG, electrocardiogram.

In Fig. 8, all hardware equipment used in the application is shown in detail. (I) represents the FPGA card, (II) represents the 16 Bit DAC, (III) represents the FPAA card.

The FPGA accelerates digital data by a factor of 1000, then converts it back to analog using the R-2R ladder DAC. The main purpose of increasing the raw data by a factor of 1000 is to shift the cutoff frequency of the applied filters to higher-frequency regions. After that, the accelerated analog data are applied as an input signal to the FPAA.

Since a single FPAA board was used in this study, it was necessary to accelerate the signal, as the cutoff frequency of the HP filter cannot be set too low (≈ 0.05Hz). The frequency of the ECG signal has increased after this process. Fig. 9 illustrates the real-time oscilloscope traces of the raw and filtered signals. Table 2 summarizes the ensemble-based signal and residual-noise powers and the corresponding SNR estimates for the raw input and filtered outputs.

IV. DISCUSSION

In addition to the time-domain comparison, an ensemble-based quantitative noise analysis was performed. The raw ECG exhibited an SNR of 16.66 dB, while the intermediate output after stages I and II exhibited an SNR of 15.49 dB. The fully filtered FPAA output achieved the highest SNR of 24.48 dB, corresponding to an improvement of 7.82 dB relative to the raw input. The BIOPAC-filtered signal exhibited an SNR of 13.89 dB. These results indicate that the complete FPAA filtering chain substantially reduced beat-to-beat residual variability under the experimental conditions.

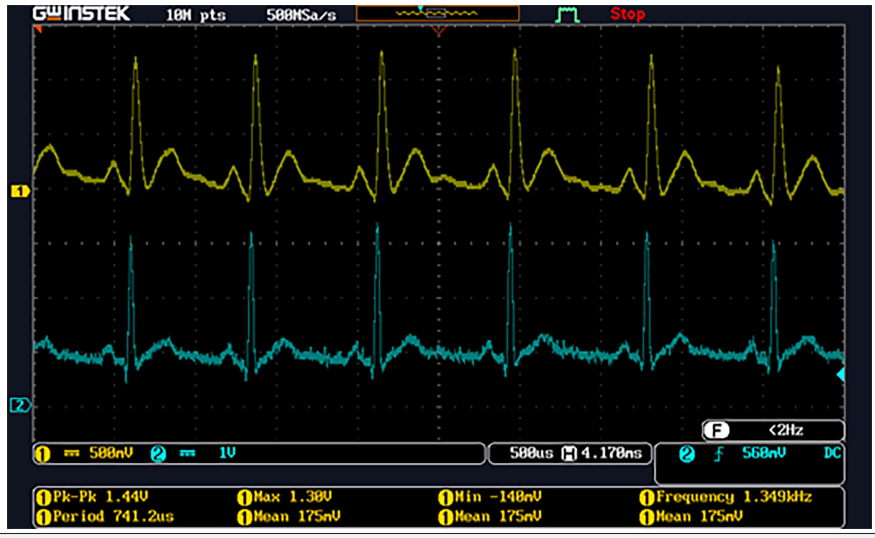


Fig. 9. Oscilloscope image of raw and filtered ECG signals. ECG, electrocardiogram.

TABLE II. ENSEMBLE-BASED SNR ANALYSIS OF THE EXPERIMENTAL ECG SIGNALS

Stage	$P_s (V^2)$	$P_n (V^2)$	SNR (dB)
Raw input	0.05531	0.001193	16.66
FPAA-intermediate output	0.05455	0.001539	15.49
FPAA-fully filtered ECG	0.02305	0.000082	24.48
BIOPAC-filtered ECG	0.04950	0.002020	13.89

ECG, electrocardiogram; FPAA, field programmable analog array; SNR, signal-to-noise ratio.

The additional third-stage FPAA filtering altered the residual-power relationship and also produced visible attenuation of the R-peak amplitude. Therefore, although the proposed architecture successfully implemented the required reconfigurable filtering functions, further optimization is required to improve the balance between noise suppression and preservation of ECG amplitude characteristics.

V. CONCLUSION

This study experimentally evaluated a reconfigurable hybrid ECG-filtering platform integrating the BIOPAC MP35, FPGA-based 1000-fold time-scale transformation, a 16-bit R-2R DAC, and an AN231E04 FPAA. The experimental measurements confirmed the functional implementation of the HP, NF, and LP filtering stages configured in AnadigmDesigner2.

The study's principal engineering contribution is the experimental realization of the BIOPAC–FPGA–DAC–FPAA processing chain and the use of FPGA-based time-scale transformation to enable very-low-frequency ECG filtering with a single FPAA device.

Future work should extend the present quantitative analysis by using controlled noise injection, independently acquired clean-reference ECG signals, repeated measurements, and additional error-based metrics.

Data Availability Statement: The data that support the findings of this study are available on request from the corresponding author.

Artificial Intelligence Usage Statement: The authors declared that no artificial intelligence tool was used in the preparation of the manuscript.

Peer-review: Externally peer-reviewed.

Author Contributions: Concept – U.C.O., F.K.; Design – U.C.O.; Supervision – F.K.; Resources – U.C.O.; Materials – U.C.O., F.K.; Data Collection and/or Processing – U.C.O.; Analysis and/or Interpretation – U.C.O., F.K.; Literature Search – U.C.O.; Writing – U.C.O.; Critical Review – F.K.

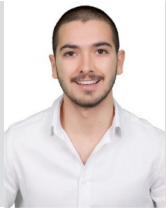
Declaration of Interests: The authors have no conflicts of interest to declare.

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